REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 5, 2006. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-5 and 18-26 are under consideration in this application. Claims 1-2, 18-21 and 25 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention.

All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claim 25 was objected to for a typing error. As indicated, claim 25 is being amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-5 and 18-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,212,777 to Gove et al. (hereinafter "Gove") in view of U.S. Patent No. 5,978,592 to Wise (hereinafter "Wise"). This rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit 1 on a semiconductor chip of the invention (for example, the embodiment depicted in Figs. 1-2, 10 & 15) comprises: a central processing unit 2 conducting a single instruction multiple data (SIMD) command; a single instruction multiple data (SIMD) unit 3 controlled by the central processing unit 2 and including a plurality of operation units conducting a concurrent operation for a plurality of data items respectively fetched therein in accordance with an interpretation result of said SIMD command by said central processing unit; a data buffer 9 connectible to said SIMD unit 3; and a data transfer control unit 5 for controlling the transfer of data between said data buffer

9 and a memory 17. The data transfer control unit 5 controls the transfer of data for a subsequent operation of the STMD unit 3 to said data buffer 9 from the memory 17 (outside of the data buffer 9) *in concurrence with* the current operation of the SIMD unit 3 for a plurality of data items read from said data buffer 9 (to internal components, such as registers 41, 42, p. 26, line 22). The data transfer control unit 5 aligns the data for the subsequent operation from the memory 17, and the aligned data for the subsequent operation is transferred to the data buffer 9 ([0009] & "*FIG. 15 shows an example in which a data aligner function is added to the data transfer controller 5.*" [0086]-[0088] of f US. Pat. App. Pub. No. 20020184471).

The data transfer control unit 5 transfers a data for a subsequent operation of the SIMD unit 3 to the buffer 9 from the memory 17 in concurrence with a current operation of the SIMD unit 3. "*The period of time used for the actual DMA transfer becomes invisible in the processing time. As a result, SIMD operation performance of the data processor 1 is increased. The SIMD operator 40 is always in a state in which necessary data with the code extension is prepared for operation.*" This increases the operational efficiency of the SIMD unit 3 (Fig. 10; [0073]), i.e., the operation of the SIMD unit 3 is not interrupted by the internal transfer of the data to the data buffer 9 ([0013] to [0017]). Therefore, the SIMD unit 3 continuously and efficiently conducts the operation.

The data for the subsequent operation from the memory 17 is aligned in the data transfer control unit 5, and the aligned data is transferred to the data buffer 9 for using the subsequent operation of the SIMD unit 3. Therefore, the SIMD unit 3 does not have to perform the data alignment operation, which is necessary in the prior art and achieved by, for example, a bit shift operation. The SIMD operation efficiency is accordingly increased due to the reduce of workload ([0088]-[0089]).

The invention recited in claim 25 is directed to the semiconductor integrated circuit 1 on a semiconductor chip of claim 1. The data transfer control unit 5 includes first data aligners 61 (Fig. 15) and bit extension units 25. The first data aligners 61 prepares data in an arbitrary pixel unit necessary for the SIMD operation for the data transfer to increase executing performance of the SIMD operation. The bit extension units 25 carries out necessary code extension in the data transfer to further increase the SIMD operation efficiency. The data buffer 9 has a first port (e.g., 9B in Figs. 2 & 15, 9A and 53 in Figs. 11 & 14) coupled to the operation units in the SIMD unit and providing the first data items to the operation units in the SIMD unit under control of the CPU 2, and a second port (e.g., 9A in Figs. 2 & 15, 9A and 53 in Figs. 11 & 14). The data transfer control unit 5 provides the **next**

first data items to the data buffer unit for ***a subsequent operation*** of the SIMD unit 3, while executing the **current** first data items by the operation unit in the SIMD unit 3.

In other words, the first data aligner 61 shifts a second data from a memory for the SIMD unit 3. The shift function of the first data aligner 61 is bit shift in 8 bits to a high-order side or a lower-order side. Therefore, by repeatedly conducting a 128-bit data input many times therein ([0021]), the first data aligner 61 aligns the second data from the memory which is extending over a 128-bit data boundary, and the data control unit 5 can transfer the first data (which is the aligned data) to the SIMD unit 3.

Applicants respectfully contend that none of the cited references teaches or suggests such a data transfer control unit 5 "which aligns the data for *the subsequent operation* from the memory 17, and the aligned data for the subsequent operation is transferred to the data buffer 9 (claim 1)" or "which includes first data aligners 61 to provide the next first data items to the data buffer unit for *a subsequent operation* of the SIMD unit 3, while executing the current first data items by the operation unit in the SIMD unit 3 (claim 25)" as in the present invention

As admitted by the Examiner (p. 9, lines 4-14 of the outstanding Office Action), Gave does not teach any data aligner align data from a memory then sending the data to a data buffer. Gave only shows that SIMD processors 100-103 (Fig. 1) are connected to crossbars 20, and the local memories 10 (M0-Mj) are also connected the crossbars 20. The crossbars 20 switch connections between the SIMD processors and the local memories. However, the crossbars 20 simply do NOT align data from any local memory to any SIMD processor.

Wise was relied upon by the Examiner to provide such teachings. However, Wise aligns data for a ***current*** operation of the SIMD unit in parallel, rather than for a ***subsequent*** operation, and than transferring the aligned data for the subsequent operation to the data buffer, as does the present invention.

Applicants contend that neither Gove, Wise, nor any other cited reference teaches or suggests each and every feature of the present invention as recited in the independent claims 1 and 25. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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